# CALL FOR PAPERS

**The 27th edition of the IEEE International Interconnect Technology Conference (IITC) will be held June 3-6, 2024 in San Jose, California.** Authors are encouraged to submit their original work describing innovative research and development in the critically important field of on-chip interconnects. The conference seeks papers on all aspects of BEOL/MOL interconnects and metallization, including design, unit process, integration and reliability. **The deadline for submission of abstracts has been extended to February 26th, 2024**.

IEEE IITC is sponsored by the IEEE Electron Devices Society as the premier conference for interconnect technology devoted to leading-edge research in the field of advanced metallization and 3D integration for ULSI IC applications. The conference seeks papers on all aspects of BEOL/MOL interconnects and metallization, including design, unit process, integration and reliability.

Applications of Interest

- Advanced interconnects: low-k interconnects, optical, wireless, and carbon-based interconnects, Airgap, 1D/2D interconnects, beyond Cu…
- Emerging BEOL Integration flows such as semi-damascene
- 3D integration & packaging concerns: Wafer-to-Wafer/Chip-to-Wafer bonding, RDL's and Interposers, Through Si Via, Non-destructive, high throughput methods to identify defects, backside power distribution network (BSPDN), thermal management
- Contacts on MOS devices: Silicide, III-V, 2D materials…
- Memory architecture: CBRAM, PCRAM, ReRAM, MRAM, FeRAM, DRAM, 3DNAND…
- Novel System and Emerging Technology: Energy harvesting, brain-inspired computing…
- Novel Form Factors: flexible electronics, wearables…

Topics of Interest

- Process integration, advanced patterning for MOL/BEOL
- Materials and Unit Processes (Dielectrics, metals, barriers, Wet, CMP, PVD, CVD, ALD, selective deposition/SAMs, patterning, advanced cleaning and surface treatment)
- Reliability and Failure analysis, characterization, techniques, and methods
- Advanced material/process characterization, system-technology & design-technology co-optimization, and modelling techniques

Abstract Information

Abstracts must be no more than 3 pages in length. Details of abstract submission, including a template may be found at https://iitc-conference.org/call-for-papers/. Submissions will be reviewed for acceptance as an oral presentation or poster. Accepted abstracts will be published digitally by IEEE as IITC Conference Proceedings without further changes.

## KEYNOTE SPEAKERS

"**Materials Challenges for the Semiconductor Industry**"
Dr. James A. O'Neill
Senior VP and CTO
Entegris

"**Technology Innovations to Fuel 1T Transistors**"
Dr. Huiming Bu
Vice President, Global Semiconductor R&D and Albany Operations
IBM Research

"**Memory Technology: Status and Scaling Perspective**"
Dr. Nirmal Ramaswamy
Vice President, Advanced DRAM and Emerging Memory Technology
Micron Technology Inc.

## WORKSHOP PROGRAM

"**New dimensions to harness, upside & backside; what to consider and how to control?**"

As CMOS scaling shifts from conventional planar-based scaling to more 3D scaling, new opportunities are being explored in the vertical dimension to continue improving power, performance, and area (PPA). This trend started with the evolution of device architectures such as FinFETs, Nanosheets, VTFETs, and StackFETs. Now, the trend continues into interconnect/BEOL by tapping the backside of the wafer (BSPDN) and by aggregating semiconductor dies vertically (HBM). Vertical integration opens doors to novel chip designs and packaging that can achieve improved PPA. However, it also brings new challenges in many areas such as wafer distortion, metrology, defect control, heat management, and reliability. It is essential to overcome these challenges to achieve manufacturability of the devices with novel structures. Dealing with issues stemming from wafer bonding and thinning is one of the key areas that is much more stringent for advanced node devices, especially for the lithography process on the wafer backside. Heat dissipation of the bonded wafers where the Si substrate is not existent is another important challenge. In this workshop, experts from the industry and academia will have a deep dive into the key technical challenges so that the audience can have a better understanding and insights on the topics.

| **Speaker** | **Affiliation** | **Theme/Title** |
|---|---|---|
| Stanley S.C. Song | Google | BSPDN design considerations for advanced logic device |
| Madhavan Swaminathan | Penn State University | Delivering Power and Removing Heat; Two challenges that could become the Achilles heel for AI Applications |
| Kunal Parekh | Micron | Advanced packaging solutions for high performance memory |
| Ilseok Son | TEL | Wafer bonding hybrid/fusion bonding |
| Michale Kubis | ASML | Backside patterning from lithography perspective: alignment, metrology, and overlay control |
| Fayaz Shaikh | LAM Research | Wafer warpage control by film deposition |